REMARKS/ARGUMENTS

This is in response to an Office action dated 11/21/2005.

Status
Claims 1-3 and 11-20 are pending
Claims 1-3 are rejected
Claims 11-20 are objected to.

Election/Restrictions

Applicant's election of Group I, claims 1-3, 11-20 in the reply filed on 5/12/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Objections

Claims 11-20 are objected to because of the following informalities:
In claim 11,

-lines 10, 17, 21, "the pattern silicon layer lacks antecedent basis.

-After the first etching step, all "the SOI layer" as recited on lines 11, 19, and last line; claim 12, line 3; claim 20, lines 4, 5 should becomes --the pattern SOI layer

Selected ones of **claims 11-20** have been amended to consistently recite "patterned SOI layer".

Claim Rejection(s) under 35 USC 102

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Chan et al.

Chan et al., figs. 1A-2Z and text in paragraphs [0035]-[0051] teach the claimed method for forming a transistor including the steps of disposing a planar platform 5 of silicon atop a support structure 3 of oxide which is atop a substrate 4 (fig. 2F); forming gate structures 12 both atop and beneath the planar platform 5 (figs. 1A); and forming source and drain diffusions 9 within the planar platform 5.

With respect to claims 2-3, figs. 1A shows the gate structure 12 which is formed beneath the planar platform 5 are smaller the planar platform 5 and are aligned with the gate structures which are formed atop the planar platform 5.

The Invention Generally

The invention is generally directed to planar pedestal multi gate device. A method of forming a transistor comprises disposing a planar platform (or pedestal, or layer) of silicon atop a support structure of oxide which is atop a substrate; forming gate structures both atop and beneath the planar platform; and forming source and drain diffusions within the planar platform. The gate structures which are formed beneath the planar platform may smaller than the planar platform,

and may be aligned with the gate structures which are formed atop the planar platform. A transistor formed by the method is also disclosed.

The 102 reference, Generally

Chan et al discloses Self-aligned double-gate MOSFET by selective epitaxy and silicon wafer bonding techniques. A structure and a method of manufacturing a double-gate metal oxide semiconductor transistor includes forming a laminated structure having a single crystal silicon channel layer and insulating oxide and nitride layers on each side of the single crystal silicon channel, forming openings in the laminated structure, forming drain and source regions in the openings, doping the drain and source regions, forming a mask over the laminated structure, removing portions of the laminated structure not protected by the mask, removing the mask and the insulating oxide and nitride layers to **leave the single crystal silicon channel layer suspended from the drain and source regions,** forming an oxide layer to cover the drain and source regions and the channel layer, and forming a double-gate conductor over the oxide layer such that the double-gate conductor includes a first conductor on a first side of the single crystal silicon channel layer and a second conductor on a second side of the single crystal silicon channel layer. More particularly,

[0035] Referring now to the drawings, and more particularly to Figures 1A-1D, the inventive structure is illustrated. More specifically, the inventive structure includes a substrate 4, such as a silicon wafer, an insulator 3, source and drain regions 9, source, drain and gate contacts 15, contact opening 14, double-gate 12, a passivation dielectric 13, a channel region 5, an insulator and a thin gate oxide 11. FIG. 1B illustrates a top view of the inventive structure. FIG. 1A illustrates a cross-sectional view drawn along line A-A in FIG. 1B and FIG. 1C is a cross-sectional view of the structure along line B-B in FIG. 1B. FIG. 1D illustrates an alternative embodiment that includes a dielectric spacer 21, which is discussed in greater detail below with respect to FIGS. 6A-6B

[0036] A preferred method of forming the foregoing structure is discussed below with respect to FIGS. 2A-2BB. Referring now to FIG. 2A, a substrate 5 and an insulator 1 are formed using conventional manufacturing and deposition techniques. For example, the substrate could comprise any common substrate, such as a single crystal silicon wafer. Similarly, the insulator 1 could be any type of insulator such as, silicon nitride, silicon dioxide and aluminum oxide. The insulator 1 could be formed (or grown) over the silicon wafer using common deposition techniques (or thermal growing techniques), such as chemical vapor deposition (CVD), physical vapor deposition (PVD), sputtering and other similar techniques. The insulator 1 preferably comprises a thermally grown silicon dioxide (SiO2) formed by a hot wall diffusion furnace. Alternatively, the dielectric layer can be formed of silicon nitride, an oxide/nitride/oxide (ONO) film, tantalum pentoxide (Ta2O5) or borophosphosilicate glass (BPSG) or any other similar dielectric. The insulator 1 can have any thickness appropriate for the specific device being manufactured and, in this example, preferably has a thickness in the range of 0.1 nm to 100 nm and preferably 2 nm.

[0037] As shown in FIG. 2B, a second insulator 2, such as silicon dioxide, aluminum oxide and preferably silicon nitride, is formed on top of the first insulator layer 1. As with the first insulator layer 1, the remaining material layers may have any thickness depending upon the design requirements and the second insulator layer preferably has a thickness in the range of 10 nm to

500 nm and preferably 100 nm.

[0038] In FIG. 2C, a thick (e.g., in the range of 10 nm to 1000 nm and preferably 300 nm) insulator layer 3, such as those discussed above (commouly referred to as a buried oxide layer, e.g., BOX), is formed, using well known techniques such as those discussed above, on top of the second insulator layer 2.

[0039] Then, as illustrated in FIG. 2C, another substrate 4, such as another single crystal silicon wafer, is bonded to the thick insulator 3 by flipping the structure 1, 2, 3, 5 over on the wafer 4, as illustrated by the arrow in FIG. 2C and using standard silicon bonding techniques such as SmartCut which is described in A. J. Auberton-Herve, IEDM Technical Digest, p. 3, 1996 and references within that paper (incorporated herein by reference) or using a boron etch stop.

[0040] The single crystal silicon (SOI) wafer 5 is thinned down to a required thickness using, for example, common planarization techniques such as chemical mechanical polishing (CMP), or oxidation and etching. In the example shown in FIG. 2D, the wafer 5 will be utilized as a channel region in a metal oxide semiconductor field effect transistor (MOSFET) and has a preferable thickness of in the range of 1 nm to 500 nm and preferably about 5 nm. The desired thickness depends on the device gate length.

[0041] In FIG. 2E, a thin insulator, such as those discussed above and preferably silicon dioxide 6 (in the range of 0.1 nm to 100 nm and preferably about 2 nm in this example) is formed on the SOI layer 5 and, as shown in FIG. 2F, a thick insulator, such as those discussed above and preferably silicon nitride 7 (in the range of 10 nm to 500 nm and preferably about 250 nm in this example), is formed on top of the silicon dioxide layer 6.

[0042] In FIG. 2G openings 8 are etched into the stack of films, with the etch stopping some distance into the buried oxide 3. The openings 8 can be formed using any well known conventional technique, such as lithographic masking and etching. For example, the stack of films could be etched using conventional means such as a dry etching using a mixture of gases which may include Cl.sub.2, O.sub.2, N.sub.2, NF.sub.3, SF.sub.6, and CF.sub.4 or any similar etchant. The masking layer is preferably formed of undoped silicon glass photoresist having a thickness in the range of between about 10 nm to 100 nm and more preferably about 30 nm. As shown in FIG. 2H, which is a top view of the structure and illustrates the cross-sectional line A-A for the view shown in FIG. 2G, the distance between the openings will become the length (Lg) of the gate of the MOSFET fabricated in this example.

[0043] In FIG. 2I epitaxial silicon 9 is grown selectively out of the single crystal SOI channel 5 to fill the openings 8. More specifically, the structure is heated to a temperature in the range of 400.degree. C. to 1200.degree. C., and the silicon is heated epitaxially grown from the channel using a growth method as described earlier. Again, FIG. 2J is a top view of the structure and illustrates the cross-sectional lines A-A from which FIG. 2I is viewed.

[0044] In FIG. 2K, the structure is planarized, again using well-known planarization techniques, such as those discussed above. As with the previous drawings, FIG. 2L illustrates a top view of the structure and the cross-sectional line A-A from which the structure shown in FIG. 2K is

viewed.

[0045] As shown in FIG. 2M, a common etching technique, such as reactive- ion-etching, is used to recess the silicon 9 in the openings 8. A dielectric 10 (such as oxide or nitride) is deposited conformally, again, using any of the deposition techniques discussed above, and subsequently etched using well known techniques, such as those discussed above, to form spacers 10. For example, anisotropic etching could be performed in a low pressure reactive ion etcher. Such etching etches the horizontal surfaces at a much higher rate (e.g., 50 times) than it etches the vertical surfaces, allowing the sidewall spacers 10 to remain after the etching process. As with the previous illustrations, FIG. 2N shows a top view of the structure shown in FIG. 2M.

[0046] In FIG. 20 an ion-implantation 32 is used to heavily dope the silicon 9 in the openings 8 to form the source and drain regions of the exemplary MOSFET transistor. A key feature of the invention is that the patterned insulator 7 comprises a self-aligned implant mask which protects the SOI channel region 5 from the ion implantation 32. Thus, the spacer 10 offsets the source/drain implant 32 from the channel region 5.

[0047] As shown in the top view of the structure in FIG. 2P, a mesa mask is formed and, as shown in FIGS. 2Q and 2R, the area not protected by the mesa mask is removed, using etching techniques, such as those discussed above, to isolate individual devices of the MOSFET device being described in this example.

[0048] In FIGS. 2S and 2T, the top nitride 7 and bottom nitride 2 are removed using common etching techniques, such as wet chemical etching (e.g., hot phosphoric acid), thereby forming a suspended silicon channel 5 bridging the doped silicon (e.g., source/drain) regions 9. As shown in FIGS. 2U and 2V, the insulator layers 1, 6 (e.g., sacrificial pad oxides) are removed using a common etching process, such as a wet chemical etch (e.g., using hydrofluoric acids).

[0049] A conformal gate quality insulator 11 (e.g., oxide) is grown or deposited (e.g., preferably thermally grown) on both the top and bottom surface of the SOI channel 5, using well known techniques, such as those discussed above, as shown in the cross-sectional and top view in FIGS. 2W and 2X.

[0050] In FIG. 2Y a conductor material 12 (e.g., metal, alloy, doped polysilicon, tungsten, copper, etc.) is conformally deposited around the gate oxide 11 to form a double-gate conductor in the MOSFET structure being discussed in this example. As shown in FIG. 2Z, a gate mask is formed over the conductor material 12. Then, a selective etch is applied to remove from the conductor material 12 not protected by the gate mask, resulting in the structure shown in FIGS. 2AA and 2BB.

[0051] To complete the final structure shown in FIGS. 1A-1C, a passivation dielectric 13 is deposited, again using conventional deposition techniques, such as those discussed above. Contact openings 14 are formed through the passivation dielectric 13 and the oxide dielectric 11 to expose the source and drain regions 9 using, for example, conventional photolithographic pattering and etching processes such as those discussed above, as shown in FIGS. 1A and 1B. Additionally, similar contact openings 14 are formed through the passivation dielectric 13 to

expose the conductive material 12, as shown in FIGS. 1B and 1C. A conductive material 15 is then deposited and subsequently patterned (again, using masking and etching techniques well known to those ordinarily skilled in the art, such as those discussed above) to form electrical contacts 15 to the source and drain 9, and the double-gate conductor 12.

Contrasting FIG. 2S of Chan with FIG 6 of the present invention, Chan's SOI layer 5 is supported at both side edges, which are not exposed. The SOI layer 106' of the invention is supported in the middle, which means that its side edges are exposed - see FIG 11.

Claim 1 is amended, as follows:

wherein the support structure is disposed beneath the planar platform;

This distinguishes the claimed invention from Chan.

In the present invention,

In FIG. 5, it can be observed that the patterned SOI layer 106' is a substantially planar element (hereinafter "pedestal", or platform) supported from beneath by (disposed atop) the standoff structure 110. An important feature of the invention, that the SOI pedestal 106', upon which the transistor will be built, is remote from the bulk silicon of the handle substrate 102. As will become evident, in this manner, **multiple gate structures can be formed on the silicon pedestal.** (specification, page 7, emphasis supplied) See also FIG. 11 showing **two gate electrodes atop the SOI layer** 106'.

In FIG. 7, it can be observed that by using a standoff structure 110, the polysilicon 120 can be formed to completely surround the channel (planar pedestal 106'). As will become evident, an advantage of the present invention over the prior art is that the planar pedestal multi-gate device can be scaled to smaller gate dimensions and thus provide more performance due to the multi-gate structure (described hereinbelow). The additional gate control is capable of terminating the drain fields thereby improving the short channel effect control. (specification, page 8)

FIG. 9 shows that two gate electrodes 130 can simultaneously be formed atop a single SOI layer 106'. The gate electrodes 130 are shown as being symmetrically disposed on the planar pedestal 106', on either side of a centerline CL. Also, the standoff structure 110 is shown as being **centered** under the planar pedestal 106'. It should be understood that this example is illustrative, and should not be interpreted as limiting. For example, the standoff structure 110 could be **off-center**. More than two gate electrodes or a single gate electrode could be formed atop the single SOI layer 106'. (specification, page 9; emphasis supplied)

The standoff structure 110 is a portion of patterned buried oxide (BOX) layer 104'. The standoff structure 110 is centered under the patterned silicon layer 106'. This "back etch" exposes a substantial (e.g., **approximately 80%**) portion of the underside of the patterned silicon layer 106', and a further portion of the top surface of the handle substrate 102. Suitable dimensions for the standoff structure 110 are 10-100 nm wide (left-to-right, as viewed) and approximately 200nm high. (specification, page 7; emphasis supplied) (The whole backside cannot be exposed, as in Chan, because of the support structure.)

In one embodiment, a large bottom (back) gate electrode 140 is formed which can be approximately the size (length and width) of the planar pedestal 106'. The gate electrode 140 under the planar pedestal (active Si area) 106' acts as a back gate to form a ground plane device. The back gate electrode wraps around the side edges of the active Si region 106'. This is shown in FIG. 10A. (specification, page 10)

An example of a final transistor device structure is shown in FIG. 11, which is based on the structure shown in FIG. 10B. An advantage of this invention is that instead of the gate (130) controlling the channel from only one side, the gate (top gate 130, plus bottom gate 140, 142 or 144) completely surrounds the Si channel 106' from all sides. This results in significantly improved short channel effect control. The Si pedestal structure 106' ideally is about the same height and width or smaller than the gate dimension. (specification, page 11)

A method of forming a transistor comprises disposing a planar platform (or pedestal, or layer) of silicon atop a support structure of oxide which is atop a substrate; forming gate structures both atop and beneath the planar platform; and forming source and drain diffusions within the planar platform. The gate structures which are formed beneath the planar platform may smaller than the planar platform, and may be aligned with the gate structures which are formed atop the planar platform. A transistor formed by the method is also disclosed. (Abstract; emphasis supplied)

Claim 1 is amended to clarify that the support structure is disposed beneath the planar platform and is now allowable.

Newly-presented **claims 21-27** depend from claim 1, and are directed to features of the invention discussed hereinabove. Being that they are dependent upon claim 1, they should also be deemed allowable.

Allowable Subject Matter

Claims 11-20 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter: None of the references of record teaches or suggests the claimed method for forming a transistor including in a third etching step, removing the buried oxide layer from under the patterned silicon layer to form a standoff structure, thereby exposing a portion of a bottom surface of the SOI layer; performing gate oxidation, thereby forming gate oxide on the exposed surfaces of the patterned SOI layer; depositing gate electrode material atop the handle substrate and covering the standoff structure as well as the patterned SOI layer.

Appropriate ones of claims 11-20 are amended herewith and should be deemed allowable.

The Office Action stated that the prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Wu et al., Chu, and Inoh disclose the formation of opposed gate transistors. Since the prior art was not cited against the claims, it has not been

discussed herein.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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